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09/927,675	08/10/2001	Guy Perry	MTI-31471	6524

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	5

DATE MAILED: 02/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,675	PERRY, GUY	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 34, 50 - 65 and 69 - 76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 34, 50 - 65 and 69 - 76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I in Paper No. 4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 5, 7 ~ 14, 16 ~ 18, 21, 28, 29, 31, 32, 34, 50, 52, 53, 55, 57 ~ 65, 69, 70, 72, 73, 75 and 76 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunaga.

Regarding claim 1, Matsunaga discloses in Fig. 3 a bond pad structure in a semiconductor device, comprising:

- a first bond pad (18 and 15b) and second bond pad (18, 14c, etc.);

- each of the bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with a lower metal layer (14c) of one of the bond pads extending underneath the upper metal layer (18) of the other of the bond pads.

Regarding claims 2 and 17, the phrase "wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer (material) between the first and second bond pads to a substrate underlying the bond pads" is functional language which does not differentiate the claimed apparatus over Matsunaga.

Regarding claim 5, Matsunaga discloses in Fig. 3 further comprising a conductive material (a structure directly above the layer 18) interconnecting the first bond pad to the second bond pad.

Regarding claim 7, Matsunaga discloses in Fig. 3 the conductive material overlies at least a portion of each of the first and second bond pads.

Regarding claim 8, Matsunaga discloses in Fig. 3 further comprising a bonding wire (19) connected to the conductive material.

Regarding claim 9, Matsunaga discloses in Fig. 3 a bond pad structure in a semiconductor device, comprising:

- a first bond pad (18 and 15b) and a second bond pad (18, 14c, etc.);
- each of the bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with a lower metal layer (14c) of one of the bond pads extending underneath the upper metal layer (18) of the other of the bond pads.

Further, the phrase "wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads" is functional language which does not differentiate the claimed apparatus over Matsunaga.

Regarding claim 10, Matsunaga discloses in Fig. 3 further comprising a conductive material (a structure directly above the layer 18) interconnecting and overlying at least a portion of the first and second bond pads.

Regarding claim 11, Matsunaga discloses in Fig. 3 a bond pad structure in a semiconductor device, comprising:

- a first bond pad (18 and 15b) and a second bond pad (18, 14c, etc.);
- each of the bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with a lower metal layer (14c) of the first bond pad extending beneath the upper metal layer (18) of the second bond pad.

Regarding claim 12, Matsunaga discloses in Fig. 3 a bond pad structure in a semiconductor device, comprising:

- a first bond pad (18 and 15b) and a second bond pad (18, 14c, etc.);
- each of the bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with a lower metal layer (14c) of the second bond pad extending beneath the upper metal layer (18) of the first bond pad.

Regarding claim 13, Matsunaga discloses in Fig. 3 a bond pad structure in a semiconductor device, comprising:

- a first bond pad (18 and 15b) interconnected to a second bond pad (18, 14c, etc.) by a conductive material (a structure directly above the layer 18);
- each of the bond pads comprising at least a lower metal layer (15b and 14c)and an upper metal layer (18);
- with a lower metal layer (14c) of one of the bond pads extending underneath the upper metal layer (18) of the other of the bond pads.

Regarding claim 14, Matsunaga discloses in Fig. 3 the conductive material overling a portion of each of the bond pads.

Regarding claims 16 and 21, Matsunaga discloses in Fig. 3 further comprising a bonding wire (19) connected to the conductive material.

Regarding claim 18, Matsunaga discloses in Fig. 3 a bond pad structure in a semiconductor device, comprising:

- a first bond pad (18 and 15b) and a second bond pad (18, 14c, etc.) positioned within a single passivation opening (between the layer 17);
- the first and second bond pads interconnected by a conductive material (a structure directly above the layer 18) overlying at least a portion of each of the bond pads; and
- each of the bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with a lower metal layer (14c) of one of the bond pads extending underneath the upper metal layer (18) of the other of the bond pads.

Regarding claim 28, Matsunaga discloses in Fig. 3 a bond pad structure in a semiconductor device, comprising:

- a first bond pad (18 and 15b) and a second bond pad (18 and 14c);
- each of the bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with a lower metal layer (14c) of one of the bond pads extending beneath the upper metal layer (18) of the other of the bond pads.

Further, the phrase "at least one of the bond pads functions to supply data, test a device, or supply various voltage levels" is functional language which does not differentiate the claimed apparatus over Matsunaga.

Regarding claim 29, the phrase "wherein the first bond pad is functional to receive and respond to a test mode signal by entering a test mode; and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to a receive and respond to operational mode signals" is functional language which does not differentiate the claimed apparatus over Matsunaga.

Regarding claims 31, 34 and 52, Matsunaga discloses in Fig. 3 the lower metal layer (14c) of the second bond pad extending beneath or underneath the upper metal layer (18) of the first bond pad.

Regarding claim 32, Matsunaga discloses in Fig. 3 a bond pad structure in a semiconductor device, comprising:

- a first bond pad (18 and 15b) and a second bond pad (18 and 14c);

- each of the first and second bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with a lower metal layer (14c) of one of the bond pads extending underneath the upper metal layer (18) of the other of the bond pads; and

Further, the phrase "the first bond pad functional to receive and respond to a test mode signal by entering a test mode; and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads functional to a receive and respond to an operational mode signals by entering an operational mode" is functional language which does not differentiate the claimed apparatus over Matsunaga.

Regarding claim 50, Matsunaga discloses in Fig. 3 an integrated circuit die, comprising:

- a first bond pad (18 and 15b) and a second bond pad (18 and 14c), the first and second bond pads being positioned within a single passivation opening (between the layer 17);
- each of the first and second bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with a lower metal layer (14c) of one of the bond pads extending underneath the upper metal layer (18) of the other of the bond pads.

Regarding claim 53, Matsunaga discloses in Fig. 3 further comprising a conductive material (a structure directly above the layer 18) interconnecting and overlying at least a portion of the first bond pad and the second bond pad.

Regarding claim 55, Matsunaga discloses in Fig. 3 further comprising a bonding wire (19) connected to at least one of the bond pads.

Regarding claim 57, the phrase "wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric material between the first and second bond pads to a substrate underlying the bond pads" is functional language which does not differentiate the claimed apparatus over Matsunaga.

Regarding claim 58, Matsunaga discloses in Fig. 3 an integrated circuit die, comprising:

- a first bond pad (18 and 15b) interconnected to a second bond pad (18 and 14c), the first and second bond pads being positioned within a single passivation opening (between the layer 17);
- each of the first and second bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with a lower metal layer (14c) of one of the bond pads extending beneath the upper metal layer (18) of the other of the bond pads;

Further, the phrase "wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads" is functional language which does not differentiate the claimed apparatus over Matsunaga.

Regarding claim 59, Matsunaga discloses in Fig. 3 the first and second bond pads being interconnected by a conductive material (a structure directly above the layer 18) interconnecting overlying and in conductive contact with at least a portion of each of the bond pads.

Regarding claim 60, Matsunaga discloses in Fig. 3 an integrated circuit die, comprising:

- a first bond pad (18 and 15b) interconnected to a second bond pad (18 and 14c), the first and second bond pads being positioned within a single passivation opening (between the layer 17);
- each of the first and second bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18); and
- the lower metal layer (14c) of the first bond pad extending beneath the upper metal layer (18) of the second bond pad.

Regarding claim 61, Matsunaga discloses in Fig. 3 an integrated circuit die, comprising:

- a first bond pad (18 and 15b) interconnected to a second bond pad (18 and 14c), the first and second bond pads being positioned within a single passivation opening (between the layer 17);
- each of the first and second bond pads comprising at least a lower metal layer (15b and 14c) and an upper metal layer (18);
- with the lower metal layer (14c) of the second bond pad extending beneath the upper metal layer (18) of the first bond pad.

Regarding claim 62, Matsunaga discloses in Fig. 3 an integrated circuit die, comprising:

- a first bond pad (18 and 15b) and a second bond pad (18 and 14c);
- each of the first and second bond pads comprising at least a lower metal layer () and an upper metal layer (18);
- the lower metal layer (14c) of one of the bond pads extending beneath the upper metal layer (18) of the other of the bond pads; and

Further, the phrase "at least one of the bond pads functional to supply data, retrieve data, test a device, or supply various voltages" is functional language which does not differentiate the claimed apparatus over Matsunaga.

Regarding claims 63 and 65, Matsunaga discloses in Fig. 3 further comprising a conductive material (a structure directly above the layer 18) interconnecting and overlying at least a portion of each of the bond pads.

Regarding claim 64, the phrase "wherein the first bond pad is functional to receive and respond to a test mode signal by entering a test mode, and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to receive and respond to an operational mode signal by entering an operational mode" is functional language which does not differentiate the claimed apparatus over Matsunaga.

Regarding claim 69, Matsunaga discloses in Fig. 3 a bond pad structure disposed on a substrate and comprising multiple bond pads, each bond pad comprising overlying upper (18) and lower (15b, 14c, etc.) metal layers, and the upper metal layer (18) of one of the bond pads overlapping the lower metal layer (14c) of another of the bond pads.

Regarding claim 70, Matsunaga discloses in Fig. 3 a bond pad structure disposed on a substrate and comprising two or more bond pads, each bond pad comprising overlying upper (18) and lower (15b, 14c, etc.) metal layers, and the upper metal layer (18) of one of the bond pads extending over the lower metal layer (14c) of another of the bond pads.

Regarding claim 72, Matsunaga discloses in Fig. 3 an integrated circuit supported by a substrate and comprising:

a bond pad structure, the bond pad structure comprising two or more bond pads, each bond pad comprising overlying upper (18) and lower (14c) metal layers, and the upper metal layer (18) of one of the bond pads extending over the lower metal layer (14c) of another of the bond pads.

Regarding claim 73, Matsunaga discloses in Fig. 3 an integrated circuit supported by a substrate and comprising:

- a first bond pad (18 and 15b) and a second bond pad (18 and 14c);
- each of the bond pads comprising a lower metal layer (15b and 14c) and an overlying upper metal layer (18); and
- the upper metal layer (18) of one of the bond pads extends beyond the lower metal layer (14c) of the one bond pad and over the lower metal layer of the other of the bond pads.

Regarding claim 75, Matsunaga discloses in Fig. 3 a semiconductor device, comprising:

- a substrate (a structure under 14b); and
- a bond pad structure disposed on the substrate, the bond pad structure comprising multiple bond pads, each bond pad comprising overlying upper (18) and lower (15b, 14c, etc.) metal layers, and the upper metal layer (18) of one of the bond pads overlaps the lower metal layer (14c) of another of the bond pads.

Regarding claim 76, Matsunaga discloses in Fig. 3 a semiconductor wafer, comprising:

- a substrate (a structure under 14b) and a bond pad structure disposed on the substrate, the bond pad structure comprising a first bond pad (18 and 15b) and a second bond pad (18, 14c, etc.);

- each of the bond pads comprising a lower metal layer (15b and 14c) and an overlying upper metal layer (18); and
- the upper metal layer (18) of one of the bond pads extends beyond the lower metal layer (14c) of the one bond pad and over the lower metal layer of the other of the bond pads.

4. Claims 22, 24, 26, 27, 71 and 74 are rejected under 35 U.S.C. 102(e) as being anticipated by Sheu et al.

Regarding claim 22, Sheu et al. discloses in Fig. 4 a bond pad structure in a semiconductor device, comprising:

- a first metal layer (404) deposited onto a substrate (400) and patterned to form first (404b) and second (404c) lower metal layer portions having a space thereinbetween;
- a dielectric layer (406) deposited over the first and second lower metal layer portions and the substrate within the space, and etched to form openings to each of the first and second lower metal layer portions; and
- a second metal layer (408) deposited over the dielectric layer and into the openings of the dielectric layer and etched to form a first (408b) and second (408c) upper metal layer portions overlying and in conductive contact with the first and second lower metal layer portions;
- the first upper (408b) and lower (404b) metal layer portions forming a first bond pad, and the second upper (408c) and lower (404c) metal layer portions forming a second bond pad;

- wherein a lower metal layer (404c) portion of one of the bond pads extends beneath the upper metal layer (408b) portion of the other of the bond pads.

Regarding claim 24, Sheu et al. discloses in Fig. 4 further comprising a conductive material (412) interconnecting the first bond pad to the second bond pad.

Regarding claim 26, Sheu et al. discloses in Fig. 4 the conductive material (412) overlies at least a portion of each of the first and second bond pads.

Regarding claim 27, Sheu et al. discloses in column 2, lines 28 ~ 30 further comprising a bonding wire connected to the conductive material.

Regarding claim 71, Sheu et al. discloses in Fig. 4 a bond pad structure disposed on a substrate and comprising:

- a lower metal layer (404) disposed on the substrate (400) and comprising first (404b) and second (404c) portions separated by a space therebetween;
- a dielectric layer (406) overlying the lower metal layer and the substrate within the space;
- one or more openings (at the place of 408a ~ 408d) extending through the dielectric layer to each of the first and second lower metal portions; and
- an upper metal layer (408) disposed over the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer;
- the upper metal layer comprising first (408b) and second (408c) portions, the first upper metal portion (408b) positioned over the first lower metal portion (404b) to

- form a first bond pad, and the second upper metal portion (408c) positioned over the second lower metal portion (404c) to form a second bond pad; and
- the upper metal portion of one of the bond pads extends over the lower metal portion of the other bond pad.

Regarding claim 74, Sheu et al. discloses in Fig. 4 an integrated circuit supported by a substrate and comprising a bond pad structure, the bond pad structure comprising:

- a lower metal layer (404) comprising first (404b) and second (404c) portions with a space therebetween;
- a dielectric layer (406) overlying the lower metal layer and within the space;
- at least one opening extending through the dielectric layer to each of the first and second lower metal portions; and
- an upper metal layer (408) overlying the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer;
- the upper metal layer (408) comprising first (408b) and second (408c) portions, the first upper metal portion positioned over the first lower metal portion to form a first bond pad, and the second upper metal portion positioned over the second lower metal portion to form a second bond pad; and
- the upper metal portion of one of the bond pads extends over the lower metal portion of the other bond pad.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 4, 30, 33, 51 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga in view of Duesman et al.

Regarding claim 3, Matsunaga discloses in Fig. 3 at least one of the lower metal layers of the one of the bond pads extends underneath the upper metal layer of the other of the bond pads.

Matsunaga does not disclose the first and second bond pads each comprising a plurality of lower metal layers. However, Duesman et al. discloses in Fig. 4a first (132A) and second (132B) bond pads each comprising a plurality of lower metal layers. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Matsunaga by using the plurality of lower metal layers as taught by Duesman et al. The ordinary artisan would have been motivated to modify Matsunaga in the manner described above for at least the purpose of decreasing the time required for signals to travel between the components (column 5, lines 56 and 57).

Regarding claim 4, Matsunaga discloses in Fig. 1 at least two lower metal layers (14b and 14c) of the one of the bond pads extend underneath the upper metal layer of the other of the bond pads.

Regarding claims 30, 33 and 51, Matsunaga discloses the claimed invention except for the lower metal layer of the first bond pad extending beneath or underneath the upper metal layer of the second bond pad. However, Duesman et al. discloses in Fig. 4a a lower metal layer (the lowest metal layer) of the first bond pad (132A) extending beneath or underneath the upper metal layer (132B) of the second bond pad. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Matsunaga by using the lower metal layer of the first bond pad as taught by Duesman et al. The ordinary artisan would have been motivated to modify Matsunaga in the manner described above for at least the purpose of decreasing the time required for signals to travel between the components (column 5, lines 56 and 57).

Regarding claim 56, Matsunaga discloses in Fig. 1 at least two lower metal layers (14b and 14c) of the one of the bond pads extend underneath the upper metal layer of the other of the bond pads.

Matsunaga does not disclose the first and second bond pads each comprising a plurality of lower metal layers. However, Duesman et al. discloses in Fig. 4a first (132A) and second (132B) bond pads each comprising a plurality of lower metal layers. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Matsunaga by using the plurality of lower metal layers as taught by Duesman et al. The ordinary artisan would have been motivated to modify Matsunaga in the manner described above for at least the purpose of decreasing the time required for signals to travel between the components (column 5, lines 56 and 57).

7. Claims 6, 15, 20 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga in view of Ohtaka et al.

Regarding claims 6, 15, 20 and 54, Matsunaga discloses the claimed invention except for the conductive material comprising a solder material or solder. However, Ohtaka et al. discloses in Fig. 1 a conductive material (4) comprising a solder material or solder. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Matsunaga by using the solder material or solder for the conductive material as taught by Ohtaka et al. The ordinary artisan would have been motivated to modify Matsunaga in the manner described above for at least the purpose of increasing the bond strength between the pads and the external device.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga.

Regarding claim 19, Matsunaga discloses the opening (between the layer 17) being formed through the passivation layer (17) to expose the bond pads.

Matsunaga does not disclose a passivation layer overlying a portion of each of the bond pads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to rearrange the passivation layer to be overlying a portion of each of the bond pads, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70. The ordinary artisan would have been motivated to modify Matsunaga in the manner described above for at least the purpose of preventing the bond pads from peeling.

9. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sheu et al. in view of Geffken et al.

Regarding claim 23. Sheu et al. discloses the claimed invention except for a passivation layer formed over the bond pads and etched to form an opening therethrough to expose the first and second bond pads. However, Geffken et al. discloses in Fig. 5 a passivation layer (130) formed over bond pads (126 and 128) and etched to form an opening (150) therethrough to expose the first and second bond pads. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Sheu et al. by using the solder material for the passivation layer as taught by Geffken et al. The ordinary artisan would have been motivated to modify Sheu et al. in the manner described above for at least the purpose of providing selectively opening to various combinations of contacts (column 4, lines 51 and 52).

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sheu et al. in view of Ohtaka et al.

Regarding claim 25, Sheu et al. discloses the claimed invention except for the conductive material comprising a solder material. However, Ohtaka et al. discloses in Fig. 1 a conductive material (4) comprising a solder material. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Sheu et al. by using the solder material for the conductive material as taught by Ohtaka et al. The ordinary artisan would have been motivated to modify Sheu et al. in the manner described above for at least the purpose of increasing the bond strength between the pads and the external device.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Suga, Wong, Sakuyama, Kim, Hubner and Yoshida disclose a pad structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
February 25, 2003

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800